



AT/62871/JAS  
PATENT

Case Docket No. MICRON.009DV1  
Date: October 30, 2001  
Page 1

In re application of : Schuegraf, et al.  
Appl. No. : 08/932,228  
Filed : September 17, 1997  
For : SHALLOW TRENCH  
ISOLATION USING LOW  
DIELECTRIC  
CONSTANT INSULATOR  
Examiner : H. Vu  
Art Unit : 2811

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Appeals and Interferences, Washington, D.C.  
20231, on

October 30, 2001

*Adeel S. Akhtar*  
(Date)  
Adeel S. Akhtar, Reg. No. 41,394

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**BOARD OF PATENT APPEALS AND INTERFERENCES  
WASHINGTON, D.C. 20231**

Sir:

Transmitted herewith in triplicate is an Appellants' Brief to the Board of Patent Appeals:

- (X) Fee for filing brief in the amount of \$320.00 is enclosed.
- (X) A check in the amount of \$320.00 to cover the foregoing fees is enclosed.
- (X) If applicant has not requested a sufficient extension of time and/or has not paid any other fee in a sufficient amount to prevent the abandonment of this application, please consider this as a Request for an Extension for the required time period and/or authorization to charge our Deposit Account No. 11-1410 for any fee which may be due. Please credit any overpayment to Deposit Account No. 11-1410.
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*Adeel S. Akhtar*  
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Schuegraf, et al. ) Group Art Unit 2811  
Appl. No. : 08/932,228 )  
Filed : September 17, 1997 )  
For : SHALLOW TRENCH )  
ISOLATION USING LOW )  
DIELECTRIC CONSTANT )  
INSULATOR )  
Examiner : H. Vu )

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October 30, 2001

*Adeel S. Akhtar*  
(Date)  
Adeel S. Akhtar, Reg. No. 41,394

**ON APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES**  
**APPELLANTS' BRIEF**

Box AF  
Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

This Appeal Brief relates to an appeal to the Board of Patent Appeals and Interferences of the final rejection set forth in an Office Action mailed June 5, 2001 in the above-captioned application.

**I. REAL PARTY IN INTEREST**

The real party in interest in this appeal is the assignee of this application, Micron Technology, Inc.

**II. RELATED APPEALS AND INTERFERENCES**

Appellants are unaware of any related appeals or interferences.

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### III. STATUS OF THE CLAIMS

The present divisional application was originally filed with Claims 11-16. Claims 21-24 were added during prosecution. Claims 11-16 and 21-24 are thus pending in the present application, and have been finally rejected in the Office Action dated June 5, 2001, which final rejection was affirmed in an Advisory Action dated August 14, 2001. Appellants filed a Notice of Appeal identifying the finally rejected Claims 11-16 and 21-24.

Accordingly, Claims 11-16 and 21-24 are the subject of this appeal. These claims are attached hereto as Appendix A.

### IV. STATUS OF AMENDMENTS

The claims before the Board appear as they were finally rejected. These pending claims are attached hereto as Appendix A.

### V. SUMMARY OF THE INVENTION

The present invention relates generally to silicon integrated circuit design technology. A variety of distinct isolation technologies with different attributes, which isolate components on integrated circuits, are known in the art. Local oxidation of silicon (LOCOS) is one example of an isolation technique that is well known by those of skill in the art. A well known drawback of LOCOS isolation is the formation of the so-called stress-induced "bird's beak" caused by oxide undergrowth, and its attendant problems. Another drawback is that LOCOS isolation results in a non-planar circuit surface.

Trench isolation is another distinct technology that can be used to isolate circuit components. The present invention pertains to *trench isolation* technology. Trench isolation technology is distinct from LOCOS and generally, is not concerned with the chronic drawbacks associated with LOCOS.

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Prior to the present invention, a drawback of basic trench isolation was the formation of voids in the trench during dielectric refill. Such voids compromise device isolation as well as the overall structural integrity. Increasing the size of the trench isolation element may decrease the voids, but it also compromises the packing density or device isolation. Embodiments of the present invention overcome void formation while providing effective device isolation by using halide-doped silicon oxide during chemical vapor deposition (CVD).

The claims at issue reflect these embodiments of the invention. Claims 21, for example, recites an isolation region that is defined by a trench within the substrate, the trench having a characteristic profile produced by an etch process. Each isolation region is also defined by a halide-doped silicon oxide filling the trench to form an isolation element. The interface between the isolation element and the substrate retains the characteristic profile or structure of the trench. Claim 11 recites an isolation structure that includes a recessed portion formed with a vertical sidewall within the semiconductor substrate and a dielectric material comprising a halide-doped silicon oxide filling the recessed portion. The dielectric material has a dielectric constant lower than the dielectric constant of silicon oxide.

## VI. ISSUES BEFORE THE BOARD

This appeal turns on two issues:

First, whether Claims 21-24 are properly rejected under 35 U.S.C. § 102(a) as being anticipated by Anjum et al. ("Anjum") (U.S. Patent No. 5,372,951). This issue turns on whether the cited reference discloses the claimed structures and features of the properly construed claims. A corollary issue is whether it is improper in determining anticipation to ignore a "process limitation" (as characterized by the Examiner) that is used as an adjective and which adequately defines the physical structure and characteristics of the device.

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Second, whether Claims 11-16 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Bose et al. ("Bose") (U.S. Patent No. 5,492,858) in view of Anjum. This issue turns on whether the cited references themselves provide any teaching, suggestion or motivation to combine, or if the Examiner incorrectly has used impermissible hindsight to find some motivation to combine.

## VII. GROUPING OF CLAIMS

For purposes of the present appeal, Claims 21, 22 and 24 stand and fall together. Claims 11-16 and 23, which are separately addressed herein, also stand and fall together. Appellants reserve the right, however, to separately argue, in subsequent continuing applications, the patentability of various dependent features not addressed herein.

## VIII. APPELLANTS' ARGUMENT

### A. Claims 21, 22, and 24 are not anticipated because Anjum et al. (U.S. Patent No. 5,372,951) fails to disclose the claimed structure.

In the Final Office Action, mailed June 5, 2001, the Examiner finally rejected Claims 21, 22, and 24 under 35 U.S.C. § 102(a) as being anticipated by Anjum et al. ("Anjum") (U.S. Patent No. 5,372,951). The Examiner argued that Anjum disclosed all of the features of Claim 21.

Anticipation under 35 U.S.C. § 102 requires the disclosure in a single piece of prior art of each and every feature of a claimed invention. *See, Apple Computer, Inc. v. Articulate Systems, Inc.*, 234 F.3d 14 (Fed. Cir. 2000). It is not enough to find that the isolation structure of Anjum can be said to reside in a "trench;" the Examiner must also show that Anjum has trench with "a characteristic profile produced by etch process." *See Applied Medical Resources Corp. v. United States Surgical Corp.*, 147 F.3d 1374, 1380 (Fed. Cir. 1998).

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Thus, in order to anticipate, Anjum must have disclosed each and every feature of Claim 21 by disclosing the identical structure. Claim 21 recites:

21. An integrated circuit having a plurality of isolation regions within a semiconductor substrate, each isolation region defined by:

a trench within the substrate, the trench having a characteristic profile produced by an etch process; and

a halide-doped silicon oxide filling the trench to form an isolation element, an interface between the isolation element and the substrate retaining the characteristic profile of the trench.

Respectfully, Appellants submit that Anjum did not disclose each and every feature of Claim 21. Specifically, Anjum failed to disclose a trench having the identical structure as the trench in Claim 21. The claim recites a "trench having a characteristic profile produced by an etch process" and moreover specifies that the filled trench in the substrate is "retaining the characteristic profile of the trench." As explained in the specification at page 2, lines 17-18, trenches resulting from etching typically are characterized by a steep sidewall profile, as compared to the resulting structure in LOCOS oxidation. Additionally, the skilled artisan would readily appreciate that such structures are different from LOCOS structures, which include a bird's beak. *See* specification at page 2, lines 17-18 and Anjum generally. Anjum disclosed a local oxidation of silicon "LOCOS" oxidation structure, which has the distinct "bird's beak" structure. *See* Anjum at col. 1, lines 51 to col. 2 line 6, and col. 5, lines 5-8. Therefore, Anjum did not anticipate because it did not disclose the trench structure of Claim 21.

The Examiner has *expressly ignored* the claim recitations, summarily concluding that they "are method recitations in a device claimed, and they are non-limiting, because only the final product is relevant, not the method of making." Final Office action at pages 2-3. The Examiner cites to M.P.E.P. § 2113 for the proposition that Appellants recite a product-by-process claim, and that the manner in which the product is made is not relevant.

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Respectfully, Appellants submit that the Examiner has misapplied the law. According to well-settled law, just because “a process limitation appears in a claim does not convert it to a product-by-process claim.” *Fromson v. Advance Offset Plate, Inc.*, 720 F.2d 1565 (Fed. Cir. 1983). So-called “process” phrases in claims are interpreted as structural limitations when they are used in an adjective, non-process sense and adequately define a physical characteristic of the product. *See Hazani v. U.S. Intern. Trade Com'n*, 126 F.3d 1473, 1479 (Fed. Cir. 1997); *In re Garner*, 412 F.2d 276, 279 (CCPA 1969); *In re Moore*, 439 F.2d 1232, 1236 (C.C.P.A. 1971); *R2 Medical Systems, Inc. v. Katecho, Inc.*, 931 F.Supp. 1397, 1425 (N.D.Ill. 1996); 2 Donald S. Chisum, *Patents* § 8.05[5], at 8-96 (1994). Examples of such phrases and words include “chemically engraved,” “etched,” “ground in place,” “expanded perlite particles which are interbonded one to another by interfusion between the surfaces thereof,” “pressfitted,” and the like. *See Hazani*, 126 F.3d at 1479; *In re Garner*, 412 F.2d at 279.

Here, the phrase “the trench having a characteristic profile produced by an etch process,” does not convert Claim 21 into a product-by-process claim. Rather, the phrase is used in an adjective, non-process sense and adequately defines a physical characteristic of the trench. In other words, the phrase simply acts as an adjective by describing the structure of the trench. The trench has the characteristic profile or structure that results from etching. Thus, the phrase is used no differently than those listed in the case law and above. Therefore, the phrase “the trench having a characteristic profile produced by an etch process,” is not a product-by-process limitation.

Similarly, the phrase “the substrate retaining the characteristic profile of the trench” does not convert the claim into a product-by-process claim. Again, the phrase describes the structure or physical characteristics of the substrate. Accordingly, Appellants submit that Claim 21 recites

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*structures* that distinguish the prior art, and therefore respectfully request withdrawal of the rejections for anticipation and allowance of the claims at issue.

The Examiner's legal proposition regarding product-by-process limitations is irrelevant in the present context. The rule about product-by-process claims applies only to the situation where the product resulting from the process is structurally identical to a product made by a prior art process. For example, the Examiner's legal propositions would apply where an applicant attempts to claim a medical drug, such as penicillin made by process X, and the prior art discloses the very same penicillin, except made by process Y. Thus, the products are structurally identical, but the processes of making are different. In such a claim, the process limitations can be considered structurally non-limiting.

However, in the instant case the products are not the same. Appellants, in Claims 21-24 are not attempting to claim an already known product though a process limitation. Therefore, the Examiner's legal propositions, including M.P.E.P. § 2113 are not applicable to the present situation. "*Once a product appearing to be substantially identical* is found and a 35 U.S.C. 102/103 rejection made, the burden shifts to the applicant to show an unobvious difference." M.P.E.P. §2113 (emphasis added). In the present application, the cited prior art does *not* appear substantially identical to the claimed structure. Figure 5 of Anjum, attached hereto as Appendix B, illustrates the product of their LOCOS process, showing a different structure than a "trench having a characteristic profile produced by an etch process." Appellants' preferred trench structure is shown in Appellants' Figure 3D, attached hereto as Appendix C.

Again, as one of skilled in the art will recognize, local oxidation of silicon (LOCOS) produces a characteristic shape including a bird's beak that is readily distinguishable, *structurally*, from the shape produced by etching a trench in silicon and filling the trench with

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silicon. The skilled artisan would thus understand the product of a trench fill process *is structurally different from* the product of a LOCOS process. The skilled artisan will readily appreciate that Appellants' claims exclude LOCOS-produced structures. In other words, Appellants' claims recite a *final product that is different* from the final product of Anjum. Compare Appendix C to Appendix B.

For all of the above-discussed reasons, Appellants respectfully assert that Claims 21, 22 and 24 are not anticipated by Anjum because Anjum failed to disclose each and every feature of the claims. Therefore, Claims 21, 22 and 24 are in a condition for allowance.

**B. Claims 11-16 and 23 are not obvious because neither reference provides any motive or suggestion to combine.**

Claims 11-16 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bose et al. ("Bose") (U.S. Patent No. 5,492,858) and Anjum. According to the Examiner, Bose disclosed an isolation structure comprising each claim feature except for "silicon oxide comprising [sic] halide doped." The Examiner asserts that Anjum disclosed an isolation structure having a halide doped silicon oxide. The Examiner summarily concludes that it would have been obvious to one of ordinary skill in the art to combine the cited references. Further, the Examiner states that "Since the halide-doped silicon oxide can be form [sic] by different processes (thermally grown, CVD, PVD, etc.), therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the trench of Bose's having the silicon oxide comprising halide-doped [sic] in order to dislodge oxygen at silicon-oxygen bond sites and to enhance thickening effect of oxide regions." Final Office Action at page 5.

To establish a *prima facie* case of obviousness there must be some suggestion or motivation, either in the references or in the knowledge generally available among those of

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ordinary skill in the art, to modify the reference. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991). “The references themselves, not the invention itself, must provide some teaching whereby the applicant’s combination would have been obvious.” *In re Gorman*, 933 F.2d 982 (Fed. Cir. 1991); *Heidelberger Druckmaschinen AG v Hantscho Commercial Products, Inc.*, 21 F.3d 1068 (Fed. Cir. 1993).

“Obviousness can not be established by hindsight combination to produce the claimed invention... [I]t is the prior art itself, and not the applicant’s achievement, that must establish the obviousness of the combination.” *In re Dance*, 160 F.3d 1339 (Fed. Cir. 1998). “Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.” *In re Dembiczaik*, 175 F.3d 994 (Fed. Cir. 1999); *see also Epochem, Inc. v. Southern California Edison Co.*, 227 F.3d 1361 (Fed. Cir. 2000).

Bose did not provide any teaching, suggestion or motivation to combine with Anjum. Bose disclosed shallow trench isolation, using a conventional silicon oxide along with a silicon nitride liner. *See Abstract* and col. 4, lines 42-44. Bose did not express any suggestion or motivation to utilize a low dielectric constant material. In fact, Bose was specifically limited to “undoped” dielectric or silicon oxide. *See* Bose, Claims 1 and 10. Moreover Bose stressed the importance of using a silicon nitride liner 18. *See* col. 5, lines 41-47. As the skilled artisan will readily appreciate, the silicon nitride liner *increased* the overall trench isolation dielectric constant in the structure of Bose, relative to a pure silicon oxide element.

Furthermore, Bose stated that shallow trench isolation avoided the drawbacks of LOCOS processing. Bose disclosed improved isolation, higher density, and minimal topographical irregularities, which contrasts with LOCOS that suffers from these very drawbacks. *See* col. 1,

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lines 19-23. Anjum specifically taught using halide-doped oxides to overcome problems in a LOCOS process, and did not disclose any advantage to such oxides' use in a non-LOCOS process. See Background of the Invention, and col. 3, lines 5-16. Accordingly, Bose would not be motivated to combine his teaching with those of Anjum because Bose was not concerned with the drawbacks of Anjum. Thus, Bose provided no suggestion or motivation to be combined with Anjum to use halide-doped silicon oxide.

Anjum failed to provide any teaching, suggestion or motivation to be combined with Bose. As mentioned previously, Bose disclosed a trench-filled structure, whereas Anjum taught a LOCOS process formed by masking and thermally oxidizing the surface of the semiconductor substrate. Anjum exclusively sought to solve problems associated with LOCOS. See col. 3, lines 5-7. The skilled artisan would not have appreciated, from the cited art, that those reasons would have application to making a trench-fill structure. Specifically, the dislodging of oxygen with fluorine at silicon-oxygen bond sites, and to enhance of the thickening effect of the oxides, was taught by Anjum as useful for reducing viscosity during thermal oxidation. See Anjum at column 4, lines 38-42. Thus, the fluorine addition was emphasized only for a thermally-grown oxide or LOCOS process. Simply stated, Anjum had no need or motivation to combine with Bose, and Bose appreciated no need to be combined with the teachings of Anjum. Therefore, Claims 11-16 are not obvious because the prior art references provide no motivation, suggestion or teaching for the asserted combination.

Further, the requisite motivation is not automatically provided by virtue of the fact that the references are from the same industry. There must be some motivation to combine found in the references themselves, which motivation is not present in this case. Here, the Examiner is using impermissible hindsight, rather than some teaching from the references themselves.

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The Examiner also states “[n]ote that a trench can be formed first, then the halide-doped silicon oxide can be form [sic] later by different processes (thermally grown, CVD, PVD) to form the LOCOS.” Final Office Action at p. 5. Presumably the Examiner refers to a known combination of trench-fill with LOCOS, sometimes referred to as “recessed LOCOS.” In this case, the asserted combination might involve etching a trench and then conducting a LOCOS process including fluorine doping (as taught by Anjum).

There are many problems with this argument from the Examiner. First, the Examiner does not provide a reference teaching recessed LOCOS that could be combined with either cited reference to teach all of the features of Claim 11. Indeed, it is highly questionable whether LOCOS would work within the silicon nitride-lined trench of Bose. Second, the Examiner has not provided any suggestion from the prior art to use the process of Anjum in a recessed LOCOS process; recessing the surface prior to oxidation already accomplishes reduction of stress, and so it is not clear that the skilled artisan would have been motivated to employ fluorine in such a process.

Third, and perhaps most importantly, conducting LOCOS on a recessed surface would not meet Appellants’ structural limitations. Such a structure would deviate from the recited “vertical sidewall” (Claim 11) and would not have an interface “retaining the characteristic profile of the trench” (Claim 21). The skilled artisan would readily have appreciated that a LOCOS process (anything more than slight oxidation of the sidewalls) would alter the sidewall structure left by a trench etch.

Because the Examiner is employing motivations that are taught only for thermally grown oxides, and applying those reasons for combining halide-doping with a trench fill process, it is evident that the Examiner is relying upon hindsight in view of the present application.

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Furthermore, the asserted combination (essentially asserting a recessed LOCOS process employing the LOCOS teachings of Anjum) would not meet the structural limitations Appellants have recited, namely a vertical sidewall and a characteristic profile left by an etch process.

Accordingly, for all of the above-mentioned reasons, Appellants request withdrawal of the rejections for obviousness, and respectfully submit that the claims are allowable over the art of record.

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## IX. CONCLUSIONS

To summarize, Appellants submits that Claims 21, 22 and 24, on appeal, are patentable because (1) independent Claim 21 recites "a trench within the substrate, the trench having a characteristic profile produced by an etch process," which is a structural feature and not a product-by-process limitation; and, (2) the cited Anjum reference did not teach each and every element of Claim 21, when the claim is properly construed to include structural features, rather than mere product-by-process limitations. Furthermore, Claims 11-16 and 23 are patentable because the Examiner has failed to provide any teaching, suggestion or motivation from the prior art to combine the asserted references. There is no motivation to combine the references absent impermissible hindsight.

## X. APPENDIX A

Attached hereto as Appendix A is a copy of the appealed claims.

## XI. APPENDIX B

Attached hereto as Appendix B is a copy of Figure 5 from the prior art reference Anjum et al., U.S. Patent No. 5,372,951.

## XII. APPENDIX C

Attached hereto as Appendix C is a copy of Figure 3D from the present application as filed.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: October 30, 2001

By: Adeel S. Akhtar

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## APPENDIX A

11. (Twice Amended) An isolation structure in a semiconductor substrate comprising:  
a recessed portion formed with a vertical sidewall within the semiconductor substrate; and  
a dielectric material comprising a halide-doped silicon oxide filling the recessed portion, said dielectric material having a dielectric constant lower than the dielectric constant of silicon dioxide.
12. (Amended) The isolation structure of Claim 11, wherein the recessed portion comprises a trench structure having a ratio of height to width of less than 2:1.
13. The isolation structure of Claim 11, wherein the recessed portion comprises a trench structure having a depth of less than 200 nm.
14. The isolation structure of Claim 11, further comprising a barrier layer disposed between the recessed portion of the semiconductor substrate and the dielectric material.
15. The isolation structure of Claim 11, wherein the dielectric material has a dielectric constant lower than 3.9.
16. The isolation structure of Claim 11, wherein the dielectric material comprises a Fluoride-doped silicon dioxide composition.
21. An integrated circuit having a plurality of isolation regions within a semiconductor substrate, each isolation region defined by:  
a trench within the substrate, the trench having a characteristic profile produced by an etch process; and  
a halide-doped silicon oxide filling the trench to form an isolation element, an interface between the isolation element and the substrate retaining the characteristic profile of the trench.
22. (Amended) The integrated circuit of Claim 21, wherein the halide-doped silicon oxide has a dielectric constant of less than 3.9.
23. The integrated circuit of Claim 21, further comprising a barrier layer disposed between the interface of the semiconductor substrate and the dielectric material.
24. The integrated circuit of Claim 21, wherein the halide-doped silicon oxide comprises fluoride-doped silicon dioxide.

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APPENDIX B

Figure 5 from Anjum et al., U.S. Patent No. 5,372,951

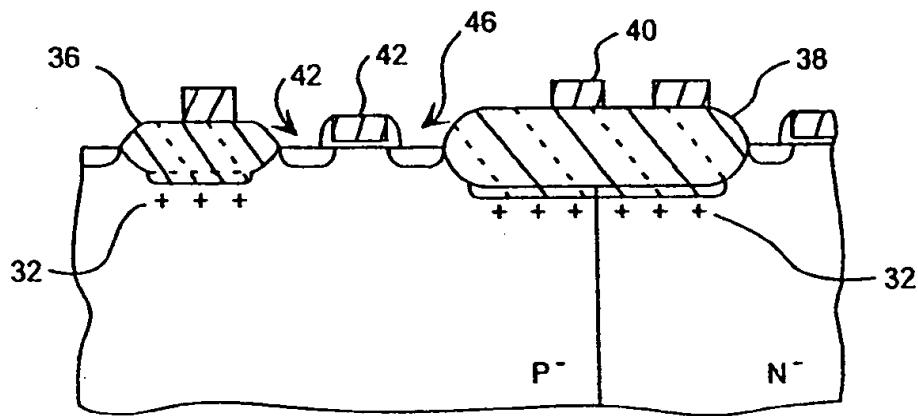


FIG. 5

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APPENDIX C

Figure 3D from the Present Application

*Fig. 3D*

